

CLAIMS

What is claimed is:

1. An integrated circuit comprising:

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a pixel sensor array having a set of pixel sensors arranged in a set of rows and a set of columns, the set of pixel sensors having a set of first color pixel sensors, a set of second color pixel sensors, and a set of third color pixel sensors;

wherein each set of color pixel sensors is configured to allow independent integration times.

2. The integrated circuit of claim 1, further comprising:

a set of reset shift registers coupled to the set of first color pixel sensors, the set of second color pixel sensors, and the set of third color pixel sensors; and,

a control unit coupled to said set of reset shift registers; wherein the control unit is configured for sequencing a set of input bits for the set of reset shift registers according to a set of desired integration times.

3. The integrated circuit of claim 1, wherein each row of pixel sensor in the set of pixel sensors has a wordline and the integrated circuit further comprising a wordline shift register coupled to each row of pixel sensors, the wordline shift register

5 having at least one output per row of pixel sensors coupled to
6 each wordline.

1 4. The integrated circuit of claim 3, where the control unit
2 further sequences a set of output bits for the wordline shift
3 register.

1 5. The integrated circuit of claim 2, where each set of color
2 pixel sensors is coupled to corresponding reset shift registers in
3 the set of reset shift registers.

1 6. The integrated circuit of claim 2, where the set of
2 integration times includes a first color integration time, a
3 second color integration time, and a third color integration time.

4 7. A method comprising:

determining a lighting environment;

determining a set of predetermined integration times based on
4 the lighting environment; and,

5 controlling a set of pixel sensors based on the set of
6 predetermined integration times, where the set of pixel sensors
7 has a first set of color pixel sensors, a second set of color
8 pixel sensors, and a third set of color pixel sensors and each set
9 of color pixel sensors has an associated integration time in the
10 set of predetermined integration times.

1 8. The method of claim 7, where controlling the set of pixel
2 sensors comprises generating a set of reset bits for placement
3 into a set of reset shift registers.

1 9. The method of claim 8, where generating a set of reset bits
2 comprises:

3 generating a set of first color reset bits for placement into
4 a first color reset shift register based on the set of
5 predetermined integration times;

6 generating a set of second color reset bits for placement
7 into a second color reset shift register based on the set of
8 predetermined integration times; and,

9 generating a set of third color reset bits for placement into
10 a third color reset shift register based on the set of
11 predetermined integration times.

1 10. The method of claim 7, further comprising reading a set of
2 pixel sensors based on the set of predetermined integration times.

1 11. The method of claim 10, where reading the set of pixel
2 sensors comprises generating a set of wordline bits for placement
3 into a wordline shift register.

1 12. An apparatus comprising:

2 means for determining a lighting environment;

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means for determining a set of predetermined integration times based on the lighting environment; and,

means for controlling a set of pixel sensors based on the set of predetermined integration times, where the set of pixel sensors has a first set of color pixel sensors, a second set of color pixel sensors, and a third set of color pixel sensors and each set of color pixel sensors has an associated integration time in the set of predetermined integration times.

13. The apparatus of claim 12, where the means for controlling the set of pixel sensors comprises a control unit configured to generate a set of reset bits for placement into a set of reset shift registers.

14. The apparatus claim 13, where the control unit comprises:

means for generating a set of first color reset bits for placement into a first color reset shift register based on the set of predetermined integration times;

means for generating a set of second color reset bits for placement into a second color reset shift register based on the set of predetermined integration times; and,

means for generating a set of third color reset bits for placement into a third color reset shift register based on the set of predetermined integration times.

1 15. The apparatus of claim 12, further comprising means for
2 reading a set of pixel sensors based on the set of predetermined
3 integration times.

1 16. The apparatus of claim 15, where the means for reading the
2 set of pixel sensors comprises a control unit configured to
3 generate a set of wordline bits for placement into a wordline
4 shift register.

1 17. An apparatus comprising:

a lens;

an integrated circuit coupled to the lens including:

5 a pixel sensor array having a set of pixel sensors
6 arranged in a set of rows and a set of columns, the set
7 of pixel sensors having a set of first color pixel
8 sensors, a set of second color pixel sensors, and a set
9 of third color pixel sensors; wherein each set of color
10 pixel sensors is configured to allow independent
integration times;

11 a system controller coupled to the integrated circuit; and,

12 a local user interface unit coupled to the system controller.

1 18. The apparatus of claim 17, further comprising:

2 a set of reset registers coupled to the set of first color
3 pixel sensors, the set of second color pixel sensors, and the set
4 of third color pixel sensors; and,

5 a control unit coupled to said set of reset shift registers;

6 wherein the control unit is configured for sequencing a set
7 of input bits for the set of reset shift registers according to a
8 set of desired integration times.

1 19. The apparatus of claim 17, wherein each row of pixel sensor
2 in the set of pixel sensors has a wordline and the integrated
3 circuit further comprising a wordline shift register coupled to
4 each row of pixel sensors, the wordline shift register having at
5 least one output per row of pixel sensors coupled to each
6 wordline.

7 20. The integrated circuit of claim 19, where the control unit
8 further sequences a set of output bits for the wordline shift
9 register.

1 21. The integrated circuit of claim 18, where each set of color
2 pixel sensors is coupled to corresponding reset registers in the
3 set of reset registers.

1 22. The integrated circuit of claim 18, where the set of
2 integration times includes a first color integration time, a
3 second color integration time, and a third color integration time.